ECL 6051				**Microwave Circuit Design**			Pre Requisites			
Version R-01							Co-requisites			
L	T	P	C	Minor Duration	Major Duration	Assignment	Minor-I Marks	Minor-II Marks	Major Marks	Total Marks
3	0	2	4	2 Hours	3 Hours	10	20	20	50	100

COURSE OUTCOMES

1. Understanding the design concept of various RF/Microwave devices.
2. Knowledge of Microwave Circuit Analysis and Impedance matching.
3. Understanding the behavior of non-linear RF/Microwave Devises.
4. Ability to design discrete RF/ Microwave Devices

COURSE CONTENTS

Unit I: Introduction: (5 contact hours)

Importance of RF Design, RF Behavior of Passive Components: High Frequency Resistors, High-Frequency Capacitors, High-Frequency Inductors. Chip Components and Circuit Board Considerations: Chip Resistors, Chip Capacitors, Surface-Mounted Inductors.

Unit II: An Overview of RF Filter Design I (5 contact hours)

Basic Resonator and Filter Configurations: Filter Type and Parameters, Low-Pass Filter, High Pass Filter, Bandpass and Bandstop Filters, Insertion Loss, Special Filter Realizations: Butterworth –Type, Chebyshev and De-normalization of Standard Low-Pass Design.

Unit III: An Overview of RF Filter Design II (5 contact hours)

Filter Implementations: Unit Elements, Kuroda's Identities and Examples of Microstrip Filter Design. Coupled Filter: Odd and Even Mode Excitation, Bandpass Filter Section, Cascading Bandpass Filter Elements, Design Examples.

Unit IV: Matching and Biasing Network (5 contact hours)

Impedance Matching using Discrete Components: Two Component Matching Networks, Forbidden regions, Frequency Response and Quality Factor, Microstrip Line Matching Networks: From Discrete Components to Microstrip Lines, Single-Stub Matching Networks, Double-Stub Matching Networks, Amplifier Classes of Operation and Biasing Network: Classes of Operation and Efficiency of Amplifiers, Bipolar Transistor Biasing Networks, Field Effect Transistor Biasing Networks.

Unit V: RF Transistor Amplifier Design I (5 contact hours)

Characteristics of Amplifiers, Amplifier Power Relations: RF source, Transducer Power Gain, Additional Power Relations, Stability Considerations: Satbility Circles, Unconditional Stability, Stabilization Methods.

Unit VI: RF Transistor Amplifier Design II (5 contact hours)

Constant Gain: Unilateral Design, Unilateral Figure of Merit, Bilateral Design, Operating and Available Power Gain Circles. Noise Figure Circles, Constant VSWR Circles. Broadband, High Power and Multistage Amplifiers.

Unit VII: RF Oscillators and Mixers (10 contact hours)

Basic Oscillator Model: Negative Resistance Oscillator, Feedback Oscillator Design, Design Steps, Quartz Oscillators. High Frequency Oscillator Configuration: Fixed Frequency Oscillators, Dielectric Resonator Oscillators, YIG-Tuned Oscillators, Voltage Controlled Oscillators, Gunn Element Oscillator. Basic Characteristics of Mixers: Basic Concepts, Frequency Domain Considerations, Single-Balanced Mixer Double-Balanced Mixer.

NOTE:	End Term Evaluation (Major Exam) shall be carried out in three stages. Minor I (20 marks), Minor II (20 marks), and Major (50 marks) exams.
	Assignment Marks shall be awarded on students' work in the form of Case Study / Design problem / Presentation / Quiz, which shall be evaluated by the concerned faculty.

Recommended Books:

Text Book :

1. RF Circuit Design Theory and Application, Reinhold Ludwig and Pavel Bretchko, Ed. 2004, Pearson Education

Reference Book:

2. Radio Frequency & Microwave Electronics Illustrated, Radmanesh, Pearson,

Microwave Circuit Design (ECL 6051)

Subject Name	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
Microwave Circuit Design (ECL 6051)	**CO1**	3	2	1	2	2	2	2	1	2	2	1	3	3	3
	CO2	3	2	3	2	2	2	2	1	2	2	1	3	2	3
	CO3	3	2	3	3	2	2	2	1	2	2	1	3	3	2
	CO4	3	2	3	3	1	3	3	2	3	2	1	3	3	2
	CO5	3	2	3	3	1	2	2	2	3	2	1	3	3	3

ECL 6170				**Optical Switching & Networks**			Pre Requisites			
Version R-01							Co-requisites			
L	T	P	C	Minor Duration	Major Duration	Assignment	Minor-I Marks	Minor-II Marks	Major Marks	Total Marks
3	0	2	4	2 Hours	3 Hours	10	20	20	50	100

Course Outcomes :

1. Recognize and classify the structures of Optical fiber and types.
2. Discuss the channel impairments like losses and dispersion (Absorption, Scattering, Material loss, Wave guide loss, Chromatic loss, Coupling Loss, PMD loss, MFD loss, Bending loss etc.)
3. Students learn about the various optical sources (LED, LASERS), detectors (PIN, APD) and fiber types and their suitability for any application
4. Familiar with Design considerations of fiber optic systems like WDM, PON, SONET/SDH etc.
5. To perform characteristics of optical fiber, sources and detectors, design as well as conduct experiments in software (OptiSystem) and hardware, analyze the results to provide valid conclusions.
6. Display a wide breadth of knowledge regarding current developments at the forefront of optical technologies (160Gbps backhaul support network, SDON, Next Generation Backhaul network)
7. Use practically, configure optimally and deploy several complex optical measurement and systems, be able to interpret systematically measurement results and evaluate errors.

Course Contents

Unit I: Optical Networking Introduction and Challenges (10 contact hours)

Advantages of optical network, telecom network overview and architecture, WDM optical networks, WDM network evolution, WDM network construction, broadcast and select optical WDM network, wavelength routed optical WDM network, Challenges of optical WDM network.

Unit II: Optical Networking Components/Building Blocks (10 contact hours)

Optical transmitters, semiconductor laser diode, tunable and fixed laser, laser characteristics, photo-detectors, tunable and fixed optical filters, channel equalizers, optical amplifiers and its characteristics, semiconductor laser amplifier, Raman amplifier, doped fiber amplifier, various switching elements, OADM, OXC, CLOS architecture, MEMS, wavelength convertors.

Unit III: Single and Multi-hop Networks (5 contact hours)

Introduction to single and multi-hop networks, Characteristics of single and multi-hop networks, experimental single hop networks: LAMBDANET, STARNET, SONATA, Rainbow, experimental multi-hop networks: Shufflenet, De Bruijn Graph, And Hypercube.

Unit IV: Optical switching (5 contact hours)

Optical packet switching basics, slotted and un-slotted networks, header and packet format, contention resolution in OPS networks, self routing, examples on OPS node architecture, optical burst switching, signaling and routing protocols for OBS networks, contention resolution in OPS networks, multicasting, implementation and application. MEMs based switching, switching with SOAs.

Unit V: Optical Access Network (5 contact hours)

Introduction to access network, PON, EPON and WDN EPON: overview, principal of operation, architecture; dynamic wavelength allocation, STARGATE: overview, need, architecture, operation and application, gigabit Ethernet, radio over fiber network.

Unit VI: Optical Multicasting and traffic grooming (5 contact hours)

Introduction to multicasting, Multicast capable switch architecture, unicast, broadcast and multicast traffic, multicast tree protection, traffic grooming overview, static and dynamic traffic grooming.

NOTE:	End Term Evaluation (Major Exam) shall be carried out in three stages. Minor I (20 marks), Minor II (20 marks), and Major (50 marks) exams.
	Assignment Marks shall be awarded on students' work in the form of Case Study / Design problem / Presentation / Quiz, which shall be evaluated by the concerned faculty.

Recommended Books:

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Optical Switching & Networks (ECL 6170)

Subject Name	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
Optical Switching & Networks (ECL 6170)	**CO1**	3	2	1	2	2	2	2	1	2	2	1	3	3	3
	CO2	3	2	3	2	2	2	2	1	2	2	1	3	2	3
	CO3	3	2	3	3	2	2	2	1	2	2	1	3	3	2
	CO4	3	2	3	3	1	3	3	2	3	2	1	3	3	2
	CO5	3	2	3	3	1	2	2	2	3	2	1	3	3	3

ECL 6070				**Synthesis & Optimization of Digital Circuits**			Pre Requisites			
Version R-01							Co-requisites			
L	T	P	C	Minor Duration	Major Duration	Assignment	Minor-I Marks	Minor-II Marks	Major Marks	Total Marks
3	0	0	3	2 Hours	3 Hours	10	20	20	50	100

COURSE OUTCOMES

1.To give theoretical background and practical skills in the area of synthesis and design of modern digital systems from high-level architectural synthesis to physical (chip) design stage.
2.Analyze the functional and nonfunctional performance of the system early in the design process to support design decisions.
3.Analyze hardware/software tradeoffs, algorithms, and architectures to optimize the system based on requirements and implementation constraints.
4.Describe architectures for control-dominated and data-dominated systems and real-time systems.
5. Understand synthesis process of EDA tools, Case studies include the architectural synthesis in DSP applications from specification to logic implementation.

COURSE CONTENTS

Unit I: Introduction: (5 contact hours)
Models for systems, characteristics of a signal processing system.

Unit II: Design Space Exploration (5 contact hours)
Introduction to the fundamental architectural synthesis problems: scheduling, allocation, binding, estimation, and control-unit synthesis

Unit III: Optimization (5 contact hours)
Introduction to graph theory and combinatorial optimization, optimization of digital signal processing systems, graph representation and annotation, mapping techniques, Optimizing timing/area.

Unit IV: Scheduling (5 contact hours)
Various scheduling techniques, scheduling algorithms, as-soon-as-possible and as-late-as-possible, list scheduling, integer linear programming.

Unit V: Binding and resource allocation (10 contact hours)
Resource sharing algorithms, interval graphs, graph colouring, integer linear program models, register sharing, Retiming, function approximation.

Unit VI: Technology Mapping and logic optimization (10 contact hours)
Technology mapping, technology libraries, cost models, graph covers, Two-level, multilevel factorization, CAD tools.

NOTE:	End Term Evaluation (Major Exam) shall be carried out in three stages. Minor I (20 marks), Minor II (20 marks), and Major (50 marks) exams.
	Assignment Marks shall be awarded on students' work in the form of Case Study / Design problem / Presentation / Quiz, which shall be evaluated by the concerned faculty.

Recommended Books:

1. Synthesis and Optimization of Digital Circuits – Giovanni De Micheli, McGraw Hill International edition,
2. Logic synthesis and verification, S. Hassoun and T. Sasao, Kluwer Academic Publishers,
3. Logic Synthsis, Srinivas Devadas et al, McGraw Hill,

Synthesis & Optimization of Digital Circuits (ECL 6070)

Subject Name	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
Synthesis & Optimization of Digital Circuits (ECL 6070)	**CO1**	3	2	1	2	2	2	2	1	2	2	1	3	3	3
	CO2	3	2	3	2	2	2	2	1	2	2	1	3	2	3
	CO3	3	2	3	3	2	2	2	1	2	2	1	3	3	2
	CO4	3	2	3	3	1	3	3	2	3	2	1	3	3	2
	CO5	3	2	3	3	1	2	2	2	3	2	1	3	3	3

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ECE XXXX			**School Elective-I**				Pre Requisites			
Version R-01							Co-requisites			
L	T	P	C	Minor Duration	Major Duration	Assignment	Minor-I Marks	Minor-II Marks	Major Marks	Total Marks
3	0	0	3	2 Hours	3 Hours	10	20	20	50	100

COURSE OUTCOMES

COURSE CONTENTS

NOTE:	End Term Evaluation (Major Exam) shall be carried out in three stages. Minor I (20 marks), Minor II (20 marks), and Major (50 marks) exams.
	Assignment Marks shall be awarded on students' work in the form of Case Study / Design problem / Presentation / Quiz, which shall be evaluated by the concerned faculty.

Recommended Books:

School Elective-I (ECE XXXX)

Subject Name	**CO**	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
School Elective-I (ECE XXXX)	**CO1**	3	2	1	2	2	2	2	1	2	2	1	3	3	3
	CO2	3	2	3	2	2	2	2	1	2	2	1	3	2	3
	CO3	3	2	3	3	2	2	2	1	2	2	1	3	3	2
	CO4	3	2	3	3	1	3	3	2	3	2	1	3	3	2
	CO5	3	2	3	3	1	2	2	2	3	2	1	3	3	3