विज्ञानं ब्रह्म

श्री माता वैष्णो देवी विश्वविद्यालय

SHRI MATA VAISHNO DEVI UNIVERSITY

Kakryal, Katra – 182320 (J&K)

(A State University Recognized u/s 2(f) & 12(B) of UGC Act, 1956)

No. SMVDU/R&D/22/9013-9018 Dated: 21 .09.2022

NOTIFICATION

Sub: List of candidates provisionally shortlisted for entrance exam and / or interview for admission to Ph.D. programme in Electronics & Communication Engineering at School of Electronics & Communication Engineering for the Odd Semester (Academic Session 2022-23) at SMVDU

The following candidates have been provisionally short listed by SRC (School Research Committees) of School of Electronics & Communication Engineering at SMVDU for Entrance Exam and / or Interview **scheduled on 27th September 2022** for admission to Ph.D. programme in Electronics & Communication Engineering at School of Electronics & Communication Engineering, SMVDU for the Odd Semester (Academic Session 2022 -23):

Sl.	Name	Parentage	Admit No.	Provisionally eligible for
1.	SUNIL KUMAR	MOHAN LAL	SOECE 101	Exempted from written exam (NET & GATE qualified)
2.	AYUSHE	ARVIND SHARMA	SOECE102	Eligible for written exam
3.	ITIKA	ROMESH KUMAR MAGOTRA	SOECE103	Eligible for written exam
4.	NEHA SHARMA (Applied for registration on part-time basis)	KULBHUSHAN KUMAR	SOECE104	Eligible for written exam

The provisionally shortlisted candidate who has qualified UGC-NET (including JRF)/UGC-CSIR NET (including JRF)/SLET/GATE/teacher-fellowship holder or has passed M.Phil is exempted from appearing in entrance written test and will directly appear in the presentation/ interview while the candidates who have not qualified these exams shall have to appear in the written test as well as interview, if qualified for the same (as per details mentioned at Sl. 3 of the general guidelines appended below). The written test and interview shall be conducted on 27TH September 2022. The candidates are hereby informed that they must report for written test and/or interview / presentation to the School of Electronics & Communication Engineering at SMVDU as per the schedule mentioned below:

Sl.	Particulars	Date and Time
1	Reporting time and document verification of all shortlisted candidates	27.09.2022 (Final timing to be intimated by the School)
2	Written Test for the candidates who have not qualified UGC-NET (including JRF)/UGC-CSIR NET (including JRF)/SLET/GATE, M.Phil or are not teacher-fellowship holder.	
3	Presentation / Interview of candidate who has qualified UGC-NET (including JRF)/UGC-CSIR NET (including JRF)/SLET/GATE/teacher-fellowship holder or has passed M.Phil.	
4	Presentation / Interview for the candidates who qualify the entrance written examination (for those candidates who have not qualified UGC-NET (including JRF)/UGC-CSIR NET (including JRF)/SLET/GATE/teacher-fellowship holder or M.Phil.)	

21/09/22.

General guidelines for the candidates

1. The result of the Written Test will be displayed on the University website www.smvdu.ac.in and on the Notice Board of the School of Electronics & Communication Engineering on 27.09.2022 in the afternoon by the Chairman, SRC of the School.
2. The Entrance written test shall consist of Multiple Choice Objective Type Questions [MCQs) of the level of Post Graduate Degree examination in the concerned subject [50% subject related and 50% Research Methodology].
3. The written test will be qualifying in nature, with 50% marks as the qualifying criteria. The candidates who qualify the written test will be required to appear for an interview/viva-voce to be conducted by the SRC of School of Electronics & Communication Engineering, where the candidates are required to discuss their research interest / area through a presentation before the SRC.
4. All provisionally shortlisted candidates must come prepared with a 10 minutes presentation (MS PPT).
5. All provisionally shortlisted candidates are required to bring all original documents and their self-attested photocopies (high school, intermediate, graduation, post-graduation, NET/SLET/GATE/M.Phil. etc.), in support of their claim as mentioned in the Ph.D. Application Form. They must carry a valid photo identification card like Adhaar / passport / government Id card / PAN card, etc.
6. Candidates in Government / Private / University services seeking admission on part time registration basis are required to submit "No Objection Certificate" obtained from their employer, at the time of written test / interview.
7. Candidates seeking admission to Ph.D. on part-time registration basis must have a minimum experience of 02 years as on date of application and must bring an "Experience Certificate" of 02 years duration. To that effect at the time of written test/interview.
8. All provisionally shortlisted candidates must submit documentary proof in respect of their claim to their eligibility in all respects on the date of written test and interview, or else they shall not be allowed to appear in the written test and interview.
9. Candidates, whose result of qualifying degree has not been declared can also appear for written test/interview. If selected and if the result of the qualifying degree of the candidate has not been declared as yet, (does not apply to cases of revaluation/re-appear etc.), the candidate may be offered provisional admission; however, the candidate is required to submit proof of having met the eligibility criteria by 15th September failing which the provisional admission will be deemed to be cancelled without any further notice and the fee submitted will be forfeited.
10. The Head of the School of Electronics & Communication Engineering shall submit the final result along with application forms and related documents (application forms with enclosures, award sheets, attendance sheet, question paper, answer key, etc) through SRC of the School and Dean of the Faculty of Engineering to R&D Section for seeking approval of the Competent Authority.
11. For any queries, Head of the School of Electronics & Communication Engineering can be contacted on 01991-285524 Extn: 2326 or email id hod.dece@smvdu.ac.in

21/09/22

Registrar

Note: No claim for TA/DA for appearing in the entrance examination / interview shall be entertained.

Copy to:

1. Dean FoE, for information.
2. Dean (R&D), for information.
3. Head SoECE, for information and compliance.
4. PS to VC for kind information of the Hon'ble Vice Chancellor.
5. I/c Website, for uploading the same on the University Website.
6. Concerned File.